ADJUSTABLE LATCHING OUTPUT OVER CURRENT CIRCUIT

Many users, for logistical reasons, employ a particular module for many applications at significantly lower power than the unit is able to provide. The potential damage to down stream PCB traces and components caused by the module high current source capability creates a need for an adjustable latching output current limit circuit.

Circuit Features:

The circuit shown in Figure 1 is intended for use with any 48V nominal DC-DC converter containing an active "LOW" shut down feature.

- SELV isolation
- No external supply needed
- 2.5V to 60V operation
- 50A limit as shown – higher currents
- achievable using different shunts and divider networks
- Few Components

Theory of Operation:

Refer to Figure 1 - The circuit is comprised of 4 essential components: A 4 wire shunt; a High Side Current Sense Amplifier; an Ultralow Power Comparator with integral reference and an Opto-Triac.

The Shunt (Rs) is connected in the + output line and is used to develop a voltage proportional to the output current flowing in the circuit. In this case a 0.001 Ohm shunt is used which results in a developed voltage range of 0 – 50mV for a corresponding 0 – 50A current flow.

This voltage is used as the input to a Current Sense Amplifier (U2) which has a fixed gain of 8. Other Gain and offsets are achievable. The output of the amplifier (0 – 400mV) is used as the non-inverting input to the comparator (U3). The inverting input of the comparator is an adjustable voltage generated from the comparator internal precision reference (1.182V ± 1%) via the divider string formed by R2 and R3. With the values for R2 and R3 as shown the voltage adjustment range is 0V to 0.394V. This input serves as the current limit reference point. Jumper J1 serves to disable the entire circuit if the full current capability of the module is desired.

Any voltage applied to the non-inverting input which is above this set reference level results in a logic "HIGH" output from the comparator.

This signal is used to drive the photodiode side of the opto-triac (U1) triggering the device. Once triggered the Triac requires typically 100µA to remain latched. The latch current is provided by the combination of R1 and D1. In the case presented the shut down port is active "LOW", i.e. pulling this pin to the –IN pin shuts off the module. Modules utilizing an active "HIGH" shut down pin will require a different arrangement of U1, R1 and D1.

The circuit should work equally well for different module input voltages provided the value of R1 is changed to maintain the recommended latch current, and that the module input voltage not exceed 400V.

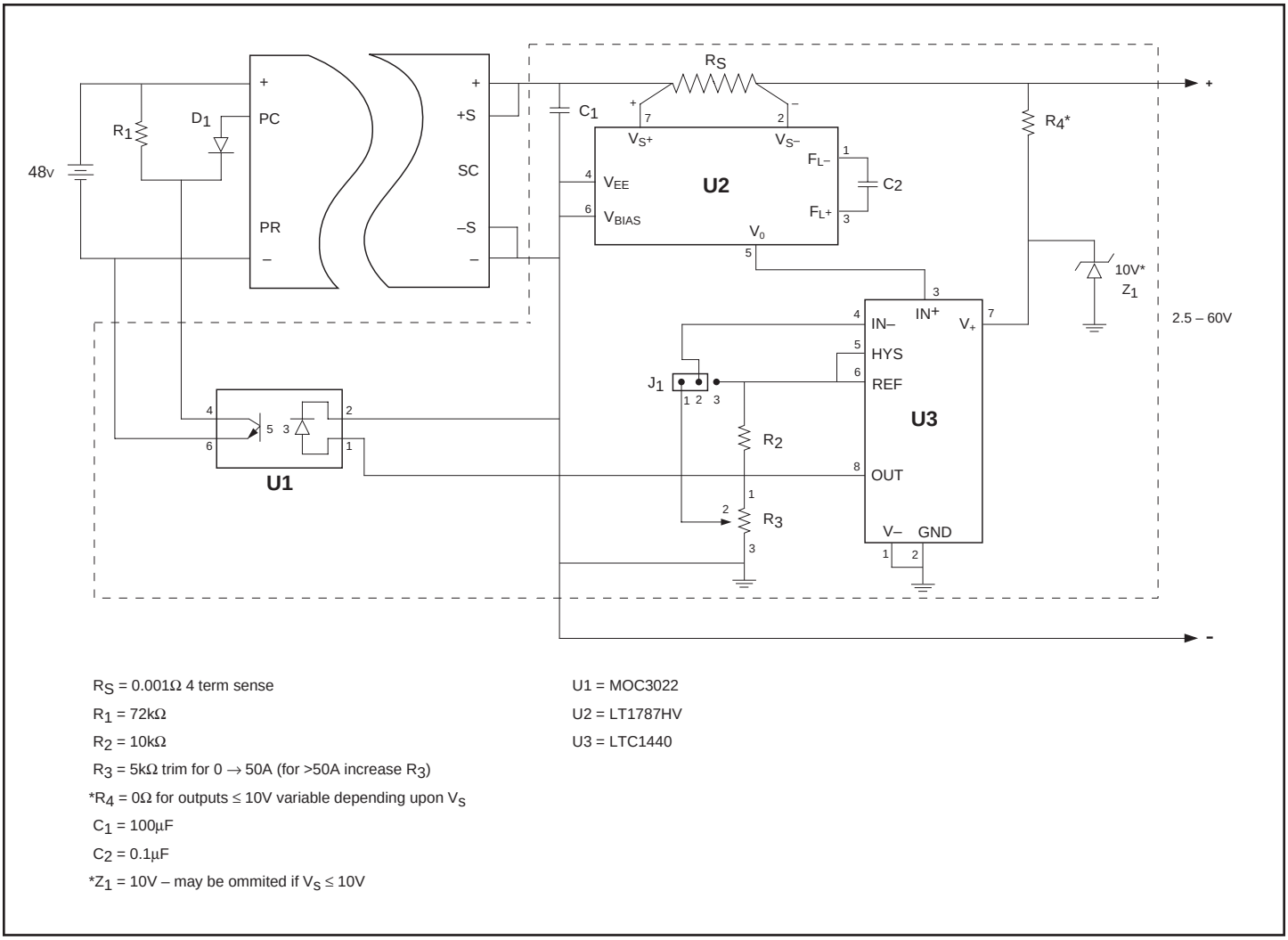
The circuit is reset by removing the module input voltage. Adding a suitably rated normally closed switch between R1 and U1 can also serve to reset the circuit.

Circuit Considerations:

As the circuit operation hinges upon the voltage developed by the shunt, care should be taken to properly connect to this device as well as providing any heat sinking that may be necessary given your specific environmental conditions.

If a short circuit is presented between the module and this circuit it will render the circuit ineffective. Also, if the short is present upon device turn on, or the impedance of the circuitry between it and the module is sufficiently low this circuit may fail to operate properly as there may not be sufficient voltage present to provide the necessary power. Testing in the lab has not shown this to be the case, nevertheless the caution remains.

U3 has an input supply range of 2V to 11V. For this reason module outputs higher than 10V should employ a V+ voltage clamp circuit for U3. This is shown in Figure 1 formed by R4 and Z1. R4 is sized to limit the current through Z1 to a safe level.

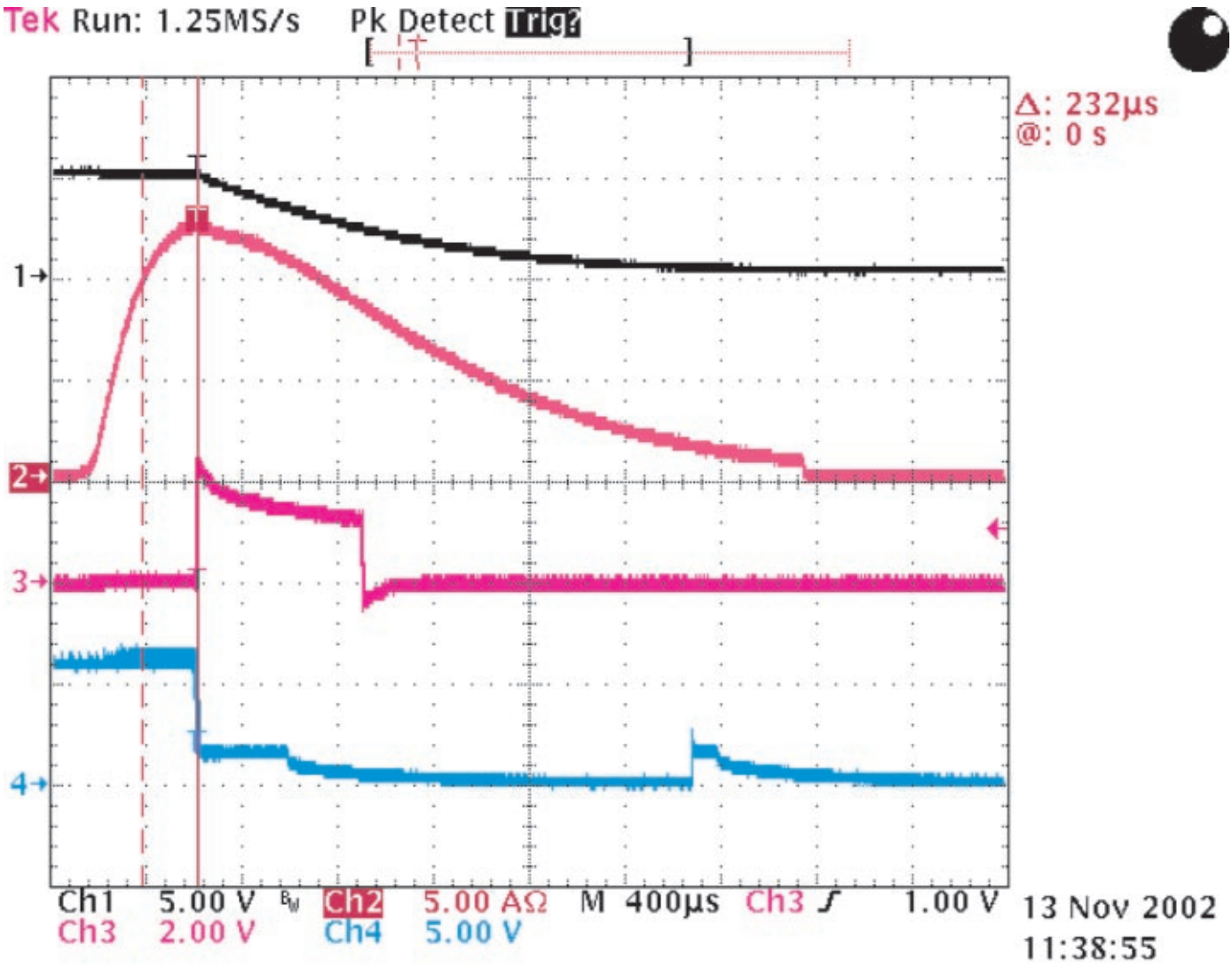


R_S = 0.001Ω 4 term sense
R_1 = 72kΩ
R_2 = 10kΩ
R_3 = 5kΩ trim for 0 → 50A (for >50A increase R_3)
*R_4 = 0Ω for outputs ≤ 10V variable depending upon V_S
C_1 = 100µF
C_2 = 0.1µF
*Z_1 = 10V – may be ommited if V_S ≤ 10V

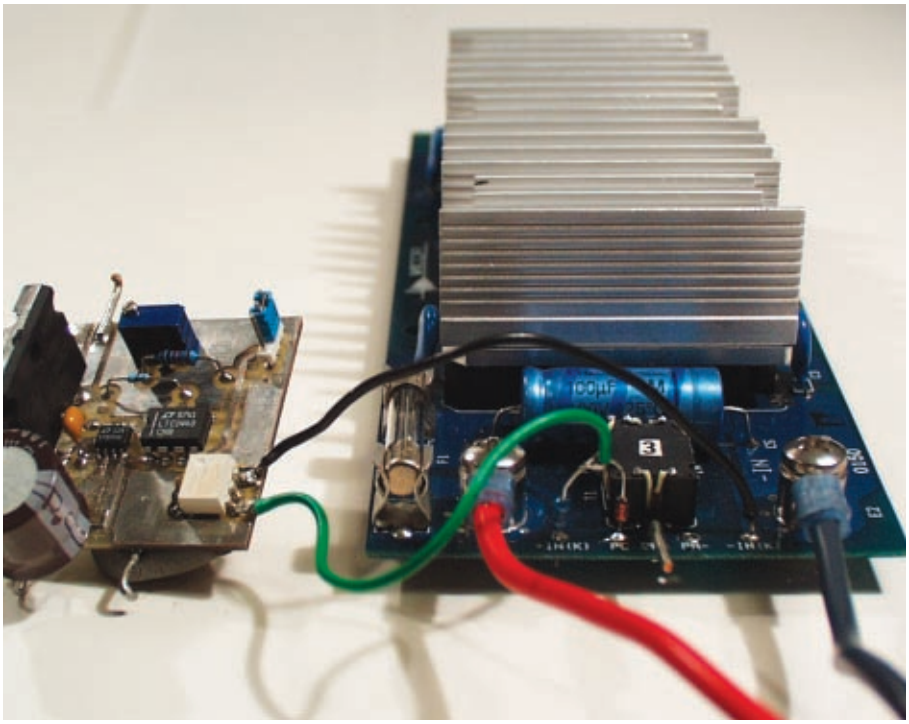
U1 = MOC3022
U2 = LT1787HV
U3 = LTC1440

Figure1.

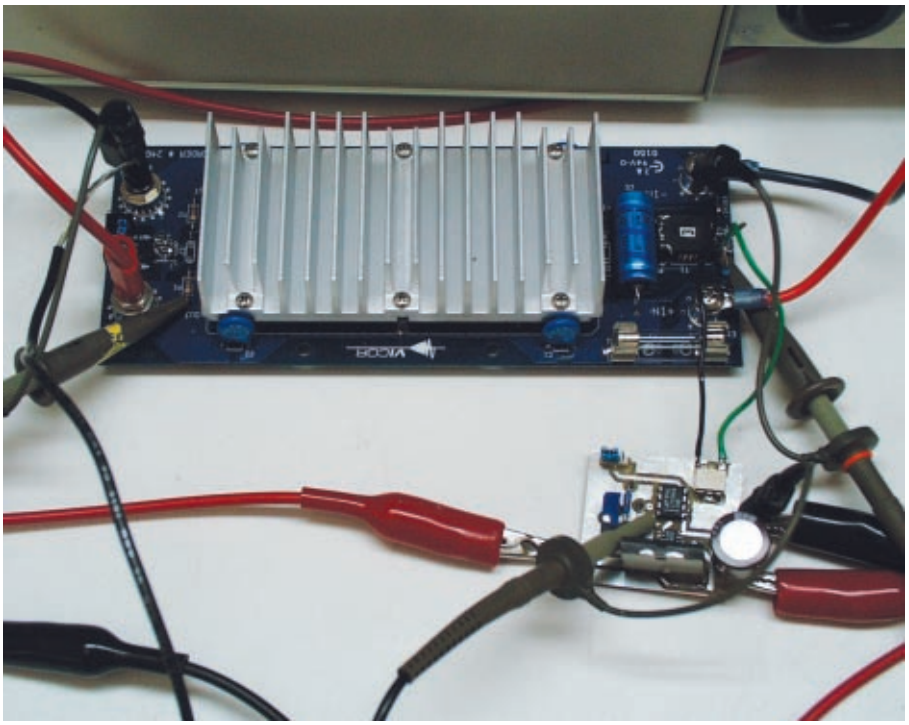
Over Current Response Timing Waveforms



Channel 1 - - Output Voltage from Module
Channel 2 - - Output Current
Channel 3 - - Output of Comparator U3 (Refer to Figure 1)
Channel 4 - - PC PIN on module
OCP Trip Threshold set for ~10A. Delay as indicated.



Breadboard and Module test vehicle.
Module is a V48A5C400A capable of sourcing in excess of 80A at 5V.
Test Circuit on Left.



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