Overview

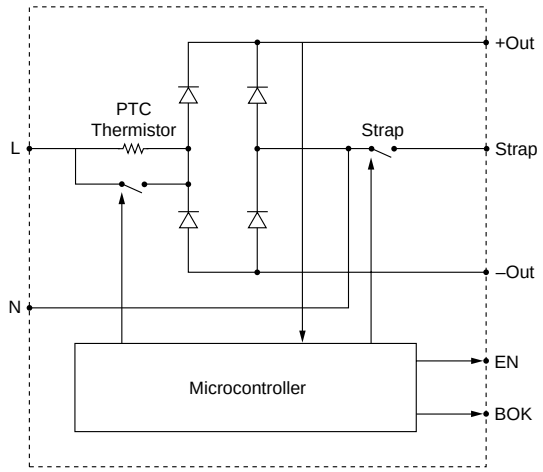
The VI-ARM (Autoranging Rectifier Module) provides an effective solution for the AC front end of a power supply built with Vicor DC-DC converters. This high performance power system building block satisfies a broad spectrum of requirements and agency standards.

The VI-ARM contains all of the power switching and control circuitry necessary for autoranging rectification, inrush current limiting, and overvoltage protection. This module also provides converter enable and status functions for orderly power up/down control or sequencing. To complete the AC front end configuration, the user needs only to add holdup capacitors and a suitable input filter with transient protection.

Functional Description

The switch that bypasses the inrush limiting PTC (positive temperature coefficient) thermistor is open when power is applied, as is the switch that engages the strap for voltage doubling. (See Figure 1.) In addition, the converter modules are disabled via the Enable (EN) line, and Bus-OK (BOK) is high.

Figure 1. Functional block diagram



Power-Up Sequence. (See Figure 2.):

1.1 Upon application of input power, the output bus capacitors begin to charge. The thermistor limits the charge current, and the exponential time constant is determined by the holdup capacitor value and the thermistor cold resistance. The slope (dv/dt) of the capacitor voltage approaches zero as the capacitors become charged to the peak of the AC line voltage.

2.1 If the bus voltage is less than 200V as the slope nears zero, the voltage doubler is activated, and the bus voltage climbs exponentially to twice the peak line voltage. If the bus voltage is greater than 200V, the doubler is not activated.

3.1 If the bus voltage is greater than 235V as the slope approaches zero, the inrush limiting thermistor is bypassed. Below 235V, it is not bypassed.

Functional Description (cont)

4.1 The converters are enabled 50 milliseconds after the thermistor bypass switch is closed.

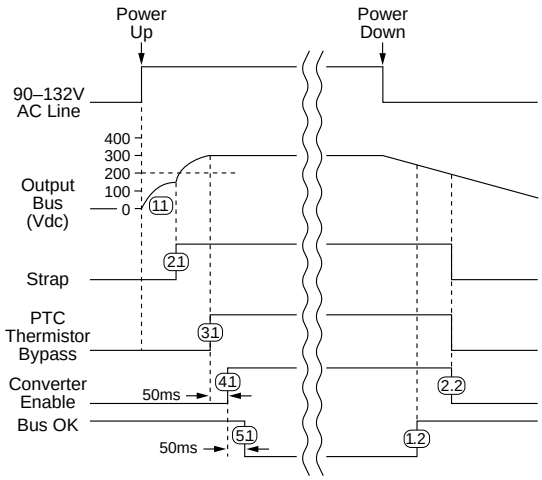
5.1 Bus-OK is asserted after an additional 50 millisecond delay to allow the converter outputs to settle within specification.

Power-Down Sequence. (See Figure 2.) When input power is turned off or fails, the following sequence occurs as the bus voltage decays:

1.2 Bus-OK is deasserted when the bus voltage falls below 210Vdc.

2.2 The converters are disabled when the bus voltage falls below 190Vdc. If power is reapplied after the converters are disabled, the entire power-up sequence is repeated. If a momentary power interruption occurs and power is reestablished before the bus reaches the disable threshold, the power-up sequence is not repeated.

Figure 2. Timing diagram: power up/down sequence



Off-Line Supply Configuration

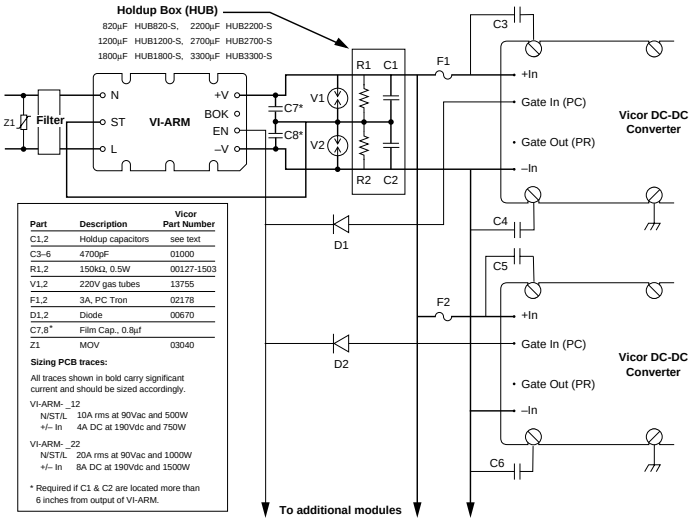
The VI-ARM maintains the DC output bus voltage between 200 and 375Vdc over the specified input range, which is compatible with Vicor VI-260 series and VI-J60 series DC-DC converters, as well as next-generation 300V input Vicor converters. The VI-ARM automatically switches to the proper rectification mode (doubled or undoubled) depending on the input voltage, eliminating the possibility of damage due to improper line connection. The VI-ARM-C12 is rated at 500W in the low range (90-132Vac input), and 750W in the high range (180-264Vac input). The VI-ARM-C22 is rated for 1000W and 1500W for the low and high input ranges, respectively. Either of these modules can serve as the AC front end for any number and combination of compatible converters as long as the maximum power rating is not exceeded.

Strap (ST) Pin. In addition to input and output power pin connections, it is necessary to connect the Strap pin to the junction of the series holdup capacitors (C1, C2, Figure 3) for

Off-Line Supply Configuration (cont)

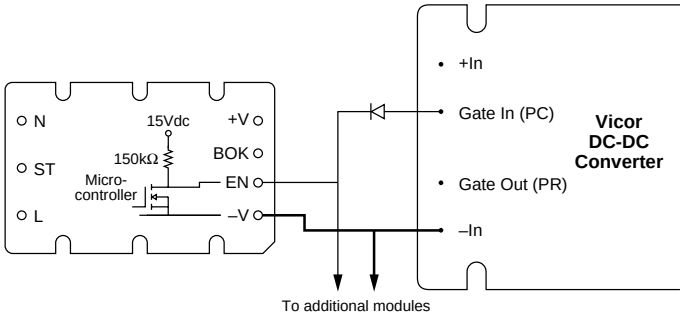
proper (autoranging) operation. Gas tubes across the capacitors provide input transient protection. The bleeder resistors (R1, R2, Figure 3) discharge the holdup capacitors when power is switched off.

Figure 3. Converter connections



Enable (EN) Pin. (See Figure 4.) The Enable pin must be connected to the Gate-In or PC pin of all converter modules to disable the converters during power-up. Otherwise, the converters would attempt to start while the holdup capacitors were being charged through an unbypassed thermistor preventing the bus voltage from reaching the thermistor bypass threshold thus disabling the power supply. The Enable output (the drain of an N channel MOSFET) is internally pulled up to 15V through a 150 kΩ resistor.

Figure 4. Enable (EN) function



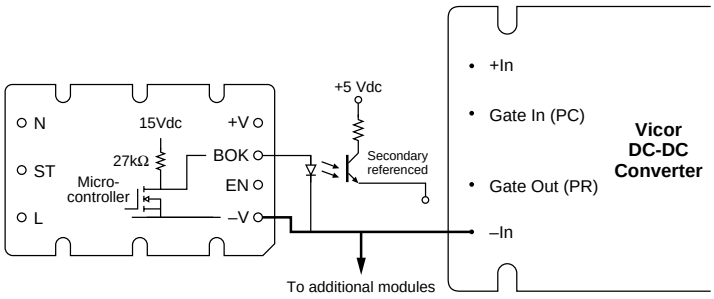
A signal diode should be placed close to and in series with the Gate-In (or PC) pin of each converter to eliminate the possibility of control interference between converters. The Enable pin switches to the high state (15V) with respect to the negative output power pin to turn on the converters after the power-up inrush is over. The Enable function also provides input overvoltage protection for the converters by turning off the converters if the DC bus voltage exceeds 400Vdc. The thermistor bypass switch opens if this condition occurs, placing the thermistor in series with the input voltage, which reduces the bus voltage to a safe level while limiting input current in case the gas tubes fire. The thermistor bypass switch also opens if a fault or overload reduces the bus voltage to less than 180Vdc.

Off-Line Power Supply Configuration (cont)

Bus-OK (BOK) Pin. (See Figure 5.) The Bus-OK pin is intended to provide early-warning power fail information and is also referenced to the negative output pin.

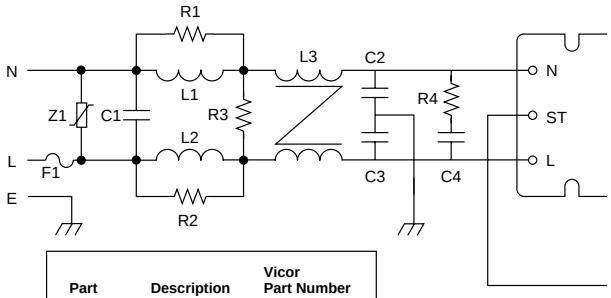
Caution: There is no input to output isolation in the VI-ARM. It is necessary to monitor Bus-OK via an optoisolator if it is to be used on the secondary (output) side of the converters. A line isolation transformation should be used when performing scope measurements. Scope probes should never be applied simultaneously to the input and output as this will destroy the unit.

Figure 5. Bus OK (BOK) isolated power status indicator



Filter. (See Figure 6.) The recommended input filter consists of a common mode choke and Y rated capacitors (line-ground) plus two additional inductors and an X rated capacitor (line-line). This filter configuration provides sufficient common mode and differential mode insertion loss in the frequency range between 100kHz and 30MHz to comply with the Level B conducted emissions limit.

Figure 6. Filter connections



Part	Description	Vicor Part Number
C1	1.0µF	02573
C2, C3	4700pF	01000
C4	0.15µF	03269
F1	12A fuse	05147
L1, L2	27µH	14563
L3	1.3mH	15016
R1, R2	10Ω	
R3	150kΩ, 0.5W	00127-1503
R4	2.2Ω	
Z1	MOV	03040

Selecting Capacitors for the VI-ARM **(Visit vicr.com for an online holdup capacitor calculator.)**

Holdup Capacitors. Holdup capacitor values should be determined according to output bus voltage ripple, power fail holdup time, and ride-through time. (See Figure 7.) Many applications require the power supply to maintain output regulation during a momentary power failure of specified duration, i.e., the converters must holdup or ride through such an event while maintaining undisturbed output voltage regulation. Similarly, many of these same systems require notification of an impending power failure in order to allow time to perform an orderly shutdown.

The energy stored on a capacitor which has been charged to voltage V is:

(1) $$\mathcal{E} = 1/2(CV^2)$$

Where: $\mathcal{E}$ = stored energy
C = capacitance
V = voltage across the capacitor

Energy is given up by the capacitors as they are discharged by the converters. The energy expended (the power-time product) is:

(2) $$\mathcal{E} = P\Delta t = C(V_1^2 - V_2^2) / 2$$

Where: P = operating power
Δt = discharge interval
V_1 = capacitor voltage at the beginning of Δt
V_2 = capacitor voltage at the end of Δt

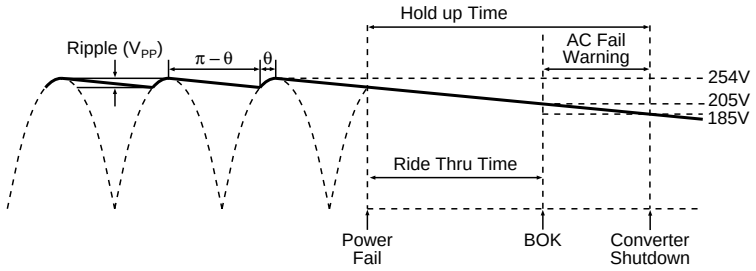
Rearranging Equation 2 to solve for the required capacitance:

(3) $$C = 2P\Delta t / (V_1^2 - V_2^2)$$

The AC fail warning time (Dt) is defined as the interval between power fail warning (BOK) and converter shutdown (EN) as illustrated in Figure 7. The Bus-OK and Enable thresholds are 205V and 185V, respectively. A simplified relationship between AC fail warning time, operating power, and bus capacitance is obtained by inserting these constants:

$$C = 2P\Delta t / (205^2 - 185^2)$$
$$C = 2P\Delta t / (7{,}800)$$

Figure 7. Holdup time



Selecting Capacitors for the VI-ARM (cont)

It should be noted that the series combination C1, C2, (Figure 3) requires each capacitor to be twice the calculated value, but the required voltage rating is reduced to 200V.

Allowable ripple voltage on the bus (or ripple current in the capacitors) may define the capacitance requirement. Consideration should be given to converter ripple rejection and resulting output ripple voltage. The ripple rejection (R) of many Vicor converters is specified as a function of the input/output voltage ratio:

(4) $$R = 30 + 20\log(V_{IN} / V_{OUT})$$

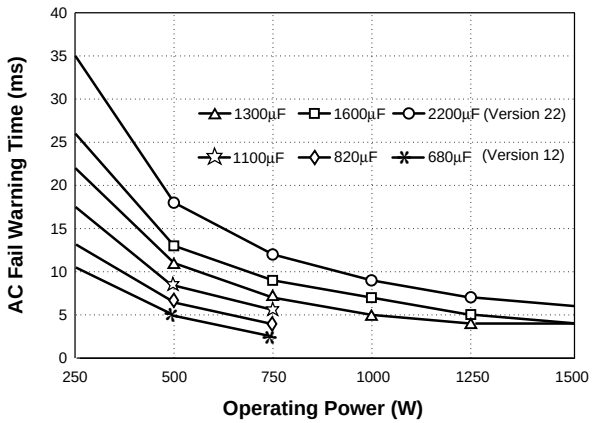


Figure 8. AC fail warning time vs. operating power and total bus capacitance, series combination on C1, C2 (Figure 3)

For example, a converter whose output is 15V and nominal input is 300V will provide 56dB ripple rejection, i.e., $10V_{PP}$ of input ripple will produce $15mV_{PP}$ of output ripple. (See Figure 11.) Equation 3 is again used to determine the required capacitance. In this case, V_1 and V_2 are the instantaneous values of bus voltage at the peaks and valleys (Figure 7) of the ripple, respectively. The capacitors must hold up the bus voltage for the time interval (Δt) between peaks of the rectified line as given by:

(5) $$\Delta t = (\pi - \theta) / 2\pi f$$

Where: f = line frequency
θ = rectifier conduction angle

The approximate conduction angle is given by:

(6) $$\theta = \text{Cos}^{-1} V_2/V_1$$

Another consideration in holdup capacitor selection is their ripple current rating. The capacitors' rating must be higher than the maximum operating ripple current. The approximate operating ripple current (rms) is given by:

(7) $$I_{RMS} = 2P/V_{ac}$$

Where: P = operating power level
V_{ac}= operating line voltage

Selecting Capacitors for the Vi-ARM (cont)

Calculated values of bus capacitance for various holdup time, ride-through time, and ripple voltage requirements are given as a function of operating power level in Figures 8, 9, and 10, respectively.

Figure 9. Hold up time vs. operating power

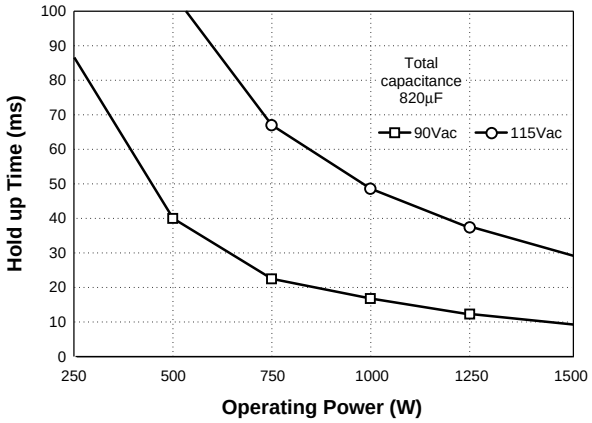
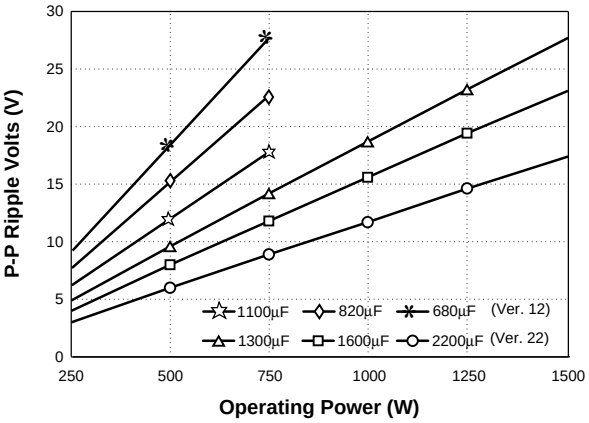


Figure 10. Ripple voltage vs. operating power and bus capacitance, series combination of C1, C2 (Figure 3)



Example

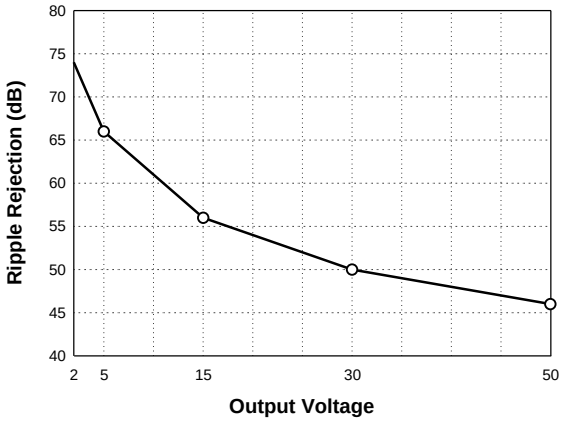
In this example, the output required at the point of load is 12Vdc at 320W. Therefore, the output power from the VI-ARM would be 375W (assuming a converter efficiency of 85%). The desired holdup time is 9 ms over an input range of 90 to 264Vac.

Determining Required Holdup Capacitance. Figure 8 is used to determine holdup capacitance for a given AC fail warning time and power level, and shows that the total bus capacitance must be at least 820 µF. Since two capacitors are used in series, each capacitor must be at least 1,640 µF. Note that AC fail warning time is not dependent on line voltage.

Selecting Capacitors for the VI-ARM (cont)

Determining Ride-through Time. Figure 9 illustrates hold up time as a function of line voltage and output power, and shows that at a nominal line of 115Vac, ride-through would be 68 ms. Hold up time is a function of line voltage.

Figure 11. Converter ripple rejection vs. output voltage



Determining Ripple Voltage on the Holdup Capacitors. Figure 10 is used to determine ripple voltage as a function of operating power and bus capacitance, and shows that the ripple voltage across the holdup capacitors will be 12Vac.

Determining the Ripple on the Output of the DC-DC Converter. Figure 11 is used to determine the ripple rejection of the DC-DC converter and indicates a ripple rejection of approximately 60 dB for a 12V output. Since the ripple on the bus voltage is 12Vac and the ripple rejection of the converter is 60 dB, the output ripple of the converter due to ripple on its input (primarily 120 Hz) will be 12 mV p-p. Note that 2nd Generation converters have greater ripple rejection than either VI-200s or VI-J00s.